

RATIONAL FREQUENCY SYNTHESIZER EMPLOYING DIGITAL **COMMUTATORS**

5

10

Inventor(s):

Ron D. Katznelson

20

- 15

Authored by:

Robert C. Strawbrich

1303 Daytona Drive

Austin, TX 78733

(512) 263-8169

(512) 263-8168 (FAX)

Express Mail Information

Express Mail Label No. EK174399614US

Date of Deposit: May 25, 2000 25

20

25

30

RATIONAL FREQUENCY SYNTHESIZER EMPLOYING DIGITAL COMMUTATORS

BACKGROUND OF THE INVENTION

It is often required to synthesize a signal source having a frequency which is a rational factor n/m times an existing reference or clock frequency. This need for synthesis may include cases where n and m are relatively prime and typical implementation of such synthesizers involves the use of phase locked loops ("PLL") operating on prescaled (divided) frequency versions of the desired signal and the reference or clock signal. These PLL synthesizers typically use a comparison frequency that is a small fraction of the reference or clock signal and thus produce synthesized signals on the desired frequency but with phase noise limitations due to frequency division. In such applications, the phase noise power is proportional to the square of the division ratio.

It is the object of the instant invention to provide for a synthesizer that permits rational synthesis, i.e. synthesis of a signal source having a frequency which is a rational factor n/m times an existing reference or clock frequency, without incurring phase noise degradations thereby providing for a signal source with phase noise essentially equal to that of the reference signal.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1 shows the first element of the preferred embodiment. A Periodic Pattern Generator 10 provides a plurality of periodic signals g_0 , g_1 through g_N where N is the number of output signals from the Periodic Pattern Generator. In the embodiment of Figure 1, a circulating shift register 12 is used to generate these signals. A "shift" signal on line 15 appears at a rate q times lower than the clock (reference) signal on line 16. Initializing the content of Shift Register 12 is accomplished by means of the Initializer Logic Control unit 11 by loading a digital bit pattern through parallel lines 14 upon the "Load" command on line 13. An alternative Periodic Pattern Generator may be

10

15

20

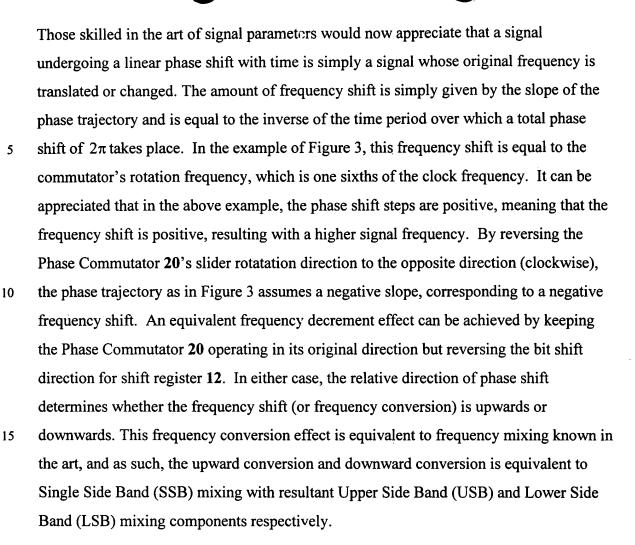
25

constructed using other means known in the art such as counters and decoders or periodic state machines having multiple taps. In an examplary embodiment of the present invention using shift register 12, a square wave pattern is initially loaded (in this case three consecutive "1's" and three consecutive "0's") although, as will be subsequently discussed, other patterns may be advantageous for certain spectral purity requirements. For the square waveform circulating in shift register 12, the resulting waveforms of the periodic signals g_0 , g_1 through g_N are shown in Figure 2. As can be seen, these are phase shifted versions of a square wave having a period of N*q times that of the reference clock signal. We refer to the frequency associated with this period as the 'shift register frequency' or the 'periodic state machine frequency' which in this case is $f_c / (Nq)$, where f_c is the reference clock frequency. The periodic signals g_0 , g_1 through g_N are fed to a Phase Commutator 20, which is an N way digital multiplexer that is controlled by MUX control lines 22 and provides an output digital signal f(t) on line 21. The periodic operation of the Phase Commutator 20 is governed by the decoded state of counter 24. Upon each clock cycle, decoder 23 decodes a different state of counter 24 and thus controls the commutator's slider to select a different signal g_i to be connected to the output line 21. If every signal line from g_0 , g_1 through g_N is selected sequentially in order, the period of the Phase Commutator 20 can be as low as N times that of the reference. If one includes in the drive of counter 24 an internal pre-divider of the reference clock by an integer p, than the Commutator 20 frequency is N*p times lower than that of the reference clock signal. We call this frequency the 'commutator frequency' which is given by f_c /(Np). Because the periodic signal's phase available to the slider of the Commutator 20 is advancing through the sequential selection of signals g_0 , g_1 through g_N , one can regard the Phase Commutator's action as providing at its output a signal f(t) with a phase which is a discrete-time step approximation to a continuous linear phase shift with time. This is shown in Figure 3 for a case in which N = 6. In reference to Figure 3, the phase trajectory of the signal f(t) is depicted as a step trajectory 30, having six equal phase steps per cycle of the Phase Commutator. It can be seen that it is a discrete time approximation to the linear phase trajectory 31 shown as a straight broken line.

30

25

30



In another mode of the preferred embodiment of the instant invention, the slider of Phase Commutator 20 may be advanced by k signal lines per each clock cycle rather than one, thereby providing the output sequence g_0 , g_k , g_{2k} , g_{3k} where the subscript index is valued modulo N. This is shown for example in Figure 3 by phase trajectory 32, which now approximates a continuous linear phase shift trajectory 33. As can be seen in this example the resultant phase slope is doubled, meaning that the conversion frequency shift is twice that related to trajectory 30. In this case there are only three phase sampling points per cycle, which degrades the quality of the approximation of a linear phase shift trajectory. However, as long as there are more than two phase samples per cycle (Nyquist Sampling Criterion), a significant energy at the intended shifted frequency will be present within the output signal f(t). However the spectral purity will be poorer than that which

10

15

20

results from a Phase Commutator having a larger number (N) of phase shifted signal lines.

A qualitative depiction of the amplitude spectrum of the output signal f(t) as a function of frequency is shown in Figure 4. The intended frequency of the output signal is shown to posses a spectral component 40, having a dominant energy component in comparison to all other components. The commutator frequency 40 is shown on a frequency scale that is centered about it for discussion purposes. The frequency scale uses integral units of the shift register frequency 42. The spectral components 43, 44,45 and 46 are due to the odd harmonic content of the square wave nature of the signals g_i provided by the Periodic Pattern Generator 10, and are related respectively to the 3rd, 5th and 7th harmonics of the square wave provided by the Periodic Pattern Generator 10. Note that other lower level spectral components 47 may be present. It can be shown mathematically that the relative levels of spectral components 47 are related to the resolution of phase increments (to the value of N) and to the relative congruence of the commutator frequency and the shift register frequency. For commutator frequencies sufficiently high compared to that of the shift register cycle, components 47 can be made progressively small with the increasing values of N. This is due to the fact that as N increases (keeping the commutator and shift register frequencies constant), the phase trajectories 30 of Figure 3 asymptotically approach the continuous linear phase trajectory 31. Of course, higher values of N would require faster clock frequencies for obtaining the same frequency at the output of the Phase Commutator. Moreover, it will be appreciated that the increase in N would also necessitate higher complexity in implementing the Periodic Pattern Generator 10 and the Phase Commutator 20.

25

30

Turning back to the resultant frequency of the output signal, based on the foregoing discussion, it should be understood that the dominant desired frequency component due to the frequency conversion is shifted by an amount equal to $f_c k s / (Nq)$ with a sign dependent on the rotation direction of the commutator and where we designate the rotation direction by the sideband value s assuming values of +1 or -1. By cascading

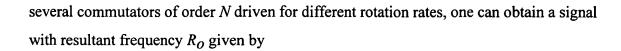
10

15

20

25

30



(1)
$$R_0 = f_c [(k_1 s_1)/q_1 + (k_2 s_2)/q_2 + ...]/N$$

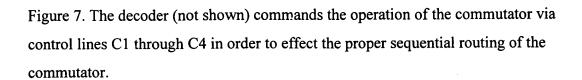
This is due to the cascaded mixing nature of the commutators. Thus, signals whose frequencies constitute a rich set of possible rational values for R_O/f_O can be generated with these structures – imparting the term Rational Synthesizer to the embodiments as described.

The Phase Commutator shown in Figure 1 has only one output. In order to provide for cascading of commutators and in order to obtain best spectral purity results, it would be advantageous to have a commutator with multiple sliders that commutate sequentially over the input signals g_{θ} , g_{I} through g_{N} and consequently provide a sequence of output signals f_0 , f_1 through f_N all having similar spectral characteristics but with different phases. In that way, cascading that well preserves the phase sampling integrity can be made possible. An example of a rational synthesizer using cascaded commutators is shown in Figure 5. In this example, Commutator Cell 2 has three inputs (N = 3) and three outputs. It is cascading Commutator Cell 1, which is a subsampled N = 6commutator running on its own independent counter. In figure 6, a cascade of two independent four way commutators (N = 4) is shown. There is considerable advantage in using four way commutators since they provide a good compromise of phase sampling resolution and implementation complexity while maintaining appreciable frequency of operation. This is because of very efficient designs available for four way digital multiplexers. Detailed description of embodiments and applications using the four way commutator-based rational synthesizers of the present invention are provided in a copending application entitled "Rational Frequency Synthesizers" filed on May 25, 2000

entirety. According to the present invention, an example of a full four-way commutator with four inputs I1, I2, I3 and I4 and having four outputs O1, O2, O3 and O4, is shown in

for the benefit of a common assignee, which is incorporated herein by this reference in its

25



Generally, for an N way rational synthesizer commutator we designate the m^{th} output signal from a commutator as a function of time by $f_m(t)$ and we note that it is periodic and thus can be represented by its Fourier spectral components which we designate as $F_m(n)$. Here, n is the harmonic index of the frequency which is n times the fundamental period. The input signals to the commutator as functions of time are designated as $g_0(t)$, $g_1(t)$ through $g_N(t)$. If these signals have more generally, not one cycle within the N stage shift register, but r complete cycles, it can be shown that the Fourier spectrum of the output signals is given by

(2)
$$F_m(n) = \frac{rNq}{2\pi(r+sq)} \exp[2\pi i smn/(qN)] \sum_{l=-\infty}^{l=\infty} \left[\frac{G(l) \exp[-2\pi i smrl/(qN)]}{rl-n} \right] H(l)$$

where H(l) is an indicator function of l given by

(3)
$$H(l) = \begin{cases} 1 & \text{whener } l(sr+q) - sn = qNu; \text{ were } u \text{ is an integer} \\ 0 & \text{otherwise} \end{cases}$$

and where G(l) is the Fourier coefficient at frequency l of the periodic signal $g_0(t)$.

By inspecting Equation (3) one notes that nonzero Fourier coefficients will only be at frequencies n for which the linear Diaphontine equation in integers l and u at the top part of the definition of H(l), has solutions. Using number theoretic tools one finds that for a square wave form of $g_0(t)$ (and hence, only odd order harmonics l) the offset frequencies n for which there is nonzero power is given by

(4) $n = \mu d + sq + r$; where d is the greatest common denominator of 2(sr+q) and qN